REMARKS

Status of Claims

Claims 1-11 are pending. Claim 1 is independent and is amended.

Rejections under 35 U.S.C. §103(a)

Applicant traverses and requests reconsideration of the rejections under 35 U.S.C. §103(a) of claims 1-6 as being obvious over U.S. Patent No. 5,440,709 to Edgar and claims 7-11 as being obvious over Edgar in view of U.S. Patent No. 4,559,618 to Houseman et al.

While not acquiescing to any rejection, but merely to advance prosecution of the present application, independent claim 1 is amended to recite a content addressable memory having a combination of elements, including a CAM control logic unit and a plurality of cells serially connected in a chain. Each cell comprises a memory which is operable, in a Search phase, to serially match a sequence of words on the common data bus with the contents of a sequence of addresses in memory blocks of the cells, the logic block being arranged for cumulatively storing the results of the matching as the matching proceeds and, in an Access phase, to render the cells matched in the Search phase serially available for access via

the common address and data buses, the Access phase occurring subsequent to the Search phase.

It is respectfully submitted that the applied art, including Edgar and Houseman et al., does not disclose or suggest the combination of elements recited in amended independent claim 1. In particular, Edgar does not disclose a comparator in combination with any of the components identified in the Office Action. While the Edgar patent states that the use of a comparator is known in conventional CAM's, all of the Edgar embodiments avoid the use of comparators. Instead, Edgar utilizes a decoding technique in lieu of performing any actual comparisons. Consequently, one of ordinary skill in the art would not have modified Edgar by flying in the face of what Edgar says not to do. Moreover, the serial operation phase shown in the fourth embodiment of Edgar does not involve matching; it is a simple memory read.

Edgar does not make the results of the successive read operations in embodiment 4 available for access via common address and data buses. The results of those read operations are confined to the internal workings of Edgar's address recognition device. There is no route for enabling those results to be coupled to any common address and/or data bus.

Edgar does not disclose rendering the results of what is termed in the Office Action a "Search phase" serially available in what the Office Action equates with an Access phase following the Search phase. In Edgar, each so-called "search" result is used immediately, before the next "search" operation. The result of each "search" is lost as soon as it has been processed. As a consequence, the result of each "search" is lost before the next "search".

Edgar does not show a Match flip-flop per cell as claim 1 now requires. As noted, Edgar does not perform any actual comparisons. Applicant fails to understand the significance of the arguments advanced in the Office Action that flip-flops are well-known in CAM's. Applicant concedes that flip-flops are well known, and there is nothing unobvious in using flip-flops in CAM's. However, Edgar fails to disclose or make obvious the specific arrangement of the flip-flops as now defined in claims 1 and 7.

Nowhere does Edgar refer to precharging circuitry or to anything that can be identified as a CAM core or a multimatch buffer. Edgar may describe his system as a CAM, but the patent does not actually show any comparison circuitry. In fact, Edgar uses look-up techniques to avoid the need for any genuine comparisons.

For at least the above reasons, it is clear that Edgar does not render obvious the combination of claim 1, upon which claims 2-11 depend. Houseman et al. does not remedy the deficiencies of Edgar as a primary reference.

With respect to claim 7, for example, since Edgar does not teach or suggest any chaining of cells as claim 1 requires, there is no motivation to apply Housesman et al. in the manner suggested in the Office Action.

More generally, the present invention is concerned with the possibility of multiple hits. The return line provides an indication that all hits have been considered. Neither Edgar nor Houseman is concerned with the possibility of multiple hits (as discussed at length in the Amendment filed June 30, 2003). In Edgar, the question does not arise, because it would be absurd for two separate components to have a common address. Since neither Edgar not Houseman has any mechanism for dealing with multiple hits, the combination of these references could scarcely generate such a mechanism.

In view of the foregoing, it is respectfully submitted that independent claim 1 is allowable. Since the remaining claims depend from allowable independent claim 1, these claims are also allowable for at least the reasons set forth above, as

well as for the additional limitations provided by these claims.

Concerning dependent claims 4-6, Applicant disagrees that the computer systems in Edgar are chained in the present sense. Applicant also disputes that Edgar shows anything which can reasonably be described as a "mask bus" as defined by claim 6. Although mask buses are known in CAM's generally, there is no need or place for masking in the Edgar structure. Masking means that some of the bits of the word being searched for are masked out so that their values are irrelevant. Edgar neither needs nor uses masking. The word "mask" does not even appear in Edgar's detailed description, and the Examiner has failed to show by scientific reasoning or evidence that Edgar inherently includes the mask bus of claim 6.

Regarding claims 8 and 11, a standard CAM includes (1) a data memory containing the words to be searched, (2) a comparator for comparing those words with a search word, and (3) some form of match registering circuitry (typically flip-flops) which records the result of the comparisons. In the present application, claims 8 and 11 disclose putting specific data in certain regions in the data memory.

In contrast to Applicant's claimed invention, Houseman et al., which is relied on in combination with Edgar to reject

claims 7-11, merely shows resetting match registering circuitry to a standard state. One of ordinary skill in the art would not find any motivation in Houseman et al. to apply match registering circuitry to data memory.

Moreover, Edgar does not disclose any identifiable data memory. As discussed, Edgar skirts this requirement (and the associated comparison circuitry) by utilizing a decoding technique which does not disclose or suggest Applicant's arrangement for putting specific data in certain regions of the data memory. There is no plausible reason for Edgar to do so.

Concerning claims 9 and 10, a key field for use of the present invention is for a data memory which can be recognized as matching a corresponding field in a search word presented to the system. Although that field forms part of the data item, it is not a key field in this sense. The Houseman et al. field is not used in matching. Rather, searching and matching is performed on a different part of the data item, and the relevant field is the desired output. Nor is it obvious to transfer this technique to Edgar, because Edgar does not have a data memory.

In view of the above amendments and remarks, it is respectfully submitted that the present application is in

condition for allowance. Favorable reconsideration is respectfully requested.

Applicant hereby requests a three-month extension of time under 37 C.F.R. §1.136. Authorization for the fee of $475 is attached. The Commissioner is hereby authorized to charge any shortage of fees, including extension of time fees, or to credit any overpayment to Deposit Account 07-1337.

Respectfully submitted,

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